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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/795,994	03/10/2004	Kazutaka Shibata	KAW 110D1	2224

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EXAMINER	
SANDVIK, BENJAMIN P	
ART UNIT	PAPER NUMBER
2826	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/29/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/795,994	SHIBATA, KAZUTAKA	
	Examiner	Art Unit	
	Ben P. Sandvik	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21,22,28-31 and 34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21,22,28-31 and 34* is/are rejected.

7)☒ Claim(s) *21 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 9/28/06
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 21 and 30 are objected to because of the following informalities: the limitation "heating up said first semiconductor chip or substrate and said second semiconductor chip to a temperature at which **said low-melting point metal layer** melts" lacks antecedent basis due to the removal of that language by the amendment. Appropriate correction is required.

Response to Arguments

Applicant's arguments with respect to claims 21 and 30 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 21 and 27 rejected under 35 U.S.C. 103(a) as being unpatentable over Dalal et al (U.S. Patent #5796591), in view of Call et al (U.S. Patent #5930597), further in view of Scharr et al (U.S. Patent #5346857), further in view of Bando et al (U.S. Patent #4592887).

With respect to **claim 21**, Dalal teaches a method for manufacturing a semiconductor device in which substrate (Fig. 5, 10) and a semiconductor chip (Fig. 5, 30) are joined to each other face-to-face via first bumps (Fig. 5, 20) provided on electrode terminals (Fig. 5, 18 and 48) of said first semiconductor chip and second bumps (Fig. 5, 38) provided on said second semiconductor chip, comprising the steps of providing at least one of said bumps with a low-melting point metal layer having a lower melting point than that of each of said bumps (Fig. 5, 41 and Col 8 Ln 49-50); heating up said first semiconductor chip or substrate and said second semiconductor chip to a temperature at which said low-melting point metal layer melts, to thereby join said substrate and semiconductor chip together (Fig. 6); and wherein one of said first bumps and corresponding second bumps is smaller in diameter than the other (Fig. 5, the first bump 20 is smaller in diameter than the second bump 38), and said first and corresponding second bumps are joined by heating such that a fillet is formed and covers at least part of a side wall of the smaller of said first and corresponding second bump (Fig. 5, 43). Dalal does not teach that the semiconductor chip and substrate are superposed without perfect alignment, that the chip and substrate are self-aligned upon heating; or filling an insulating resin into a gap between said first semiconductor chip or substrate and said second semiconductor chip after they are joined. Call teaches that a chip and semiconductor are misaligned, and then self-align upon the heating and melting of solder bumps (Col 1 Ln 42-46). It would have been obvious to one of ordinary

skill in the art at the time the invention was made to have the bumps of Dalal self-align as taught by Call in order to compensate for the chip's misalignment. Call teaches filling an insulating resin into a gap between the chip and the substrate (Fig. 3, 16). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a resin underfill as taught by Call in order to strengthen the package.

Furthermore, Dalal does not teach that at least one of said first or second bumps is a tin layer having a thickness of about 0.1 to 4 micrometers, said at least one of said first or second bumps being made of gold. Scharr teaches a tin layer having a thickness between 0.1 to 4 micrometers (Col 2 Ln 53), and that at least one of a first and second bump is made of gold (Fig. 2, 28). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a bump of gold and a tin layer of 0.1 to 4 micrometers as taught by Scharr in order to form a gold-tin eutectic, which does not compromise the high frequency performance of the device (Col 4 Ln 5).

Furthermore, Dalal and Call do not teach that said insulating resin has a thermal shrinkage factor of 4% or less. Bando teaches a thermosetting setting resin having a shrinkage factor of 3% (Col 3 Ln 56). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a resin having a thermal shrinkage factor of 4% or less as taught by Bando in order to avoid volume reduction upon curing.

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dalal, Call, Scharr, Bando, in view of Davis et al (U.S. Patent #5421507).

With respect to **claims 22**, Dalal and Call do not teach liquefying said low-melting point metal layer to thereby diffuse metals of said bumps provided on the surface of said electrode terminal into the liquefied low-melting point metal, by the liquid-phase diffusion method, thus joining said substrate and said semiconductor chip to each other, or that said low-melting point layer is made of an Au-Sn alloy or Sn. Davis teaches a method in which a low-melting point layer is liquefied to thereby diffuse said metals into the liquefied low-melting point metal, by the liquid-phase diffusion method, thus joining said substrate and said semiconductor chip together, and an interface where two Au layers are provided on copper with a layer of Sn provided between the two Au layers (Fig. 5A, 5B, 5C). It would have been obvious to one of ordinary skill in the art at the time the invention was made to join the substrate and semiconductor chip of Dalal using the liquid-phase diffusion method of Davis in order to create a high performance bond, and to select Sn as the low-melting point layer in order to take advantage of its reactive properties with Au.

Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dalal, Call, Scharr, and Bando, in view of Yamada et al (U.S. Patent #5864178), further in view of the admitted prior art in the applicant's specification.

With respect to **claim 28**, Dalal teaches gold bumps (Col 8 Ln 55), but Dalal and Call do not teach that said insulating resin and said first and second bumps have approximately the same elastic modulus. Yamada teaches a polyimide resin (Col 22 Ln 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a resin in the device of Dalal as taught by Yamada in order to reduce the mechanical stress in the device. Furthermore, the applicant's specification discloses that polyimide resin has approximately the same elastic modulus as gold bumps (Paragraph 80). It would have been obvious to one of ordinary skill in the art to have first and second bumps having approximately the same elastic modulus of the insulating resin because it is a normal property of each material.

Claims 29, 30, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dalal, Call, Scharr, and Bando, in view of Akamatsu et al (U.S. Patent #5611481).

With respect to **claim 29**, Dalal teaches that said first and second bumps are oriented toward one another in said superposing step, the end of the smaller of said first (Fig. 5, 20) and corresponding second bumps being smaller in area than the end of the larger of said first and corresponding second bumps (Fig. 5, 38), but does not teach that said first and corresponding second bumps have ends that are substantially flat. Akamatsu teaches first and second bumps having ends that are substantially flat (Fig. 1, 3 and 4). It would have been

obvious to one of ordinary skill in the art at the time the invention was made to provide flat ends on the bumps of Dalal as taught by Akamatsu in order to ensure that the electrical connection has a low contact resistance and is free from repellency problems.

With respect to **claim 30**, Dalal teaches a method for manufacturing a semiconductor device in which substrate (Fig. 5, 10) and a semiconductor chip (Fig. 5, 30) are joined to each other face-to-face via first bumps (Fig. 5, 20) provided on electrode terminals (Fig. 5, 18 and 48) of said first semiconductor chip and second bumps (Fig. 5, 38) provided on said second semiconductor chip; providing at least one of said bumps with a low-melting point metal layer having a lower melting point than that of each of said bumps (Fig. 5, 41 and Col 8 Ln 49-50); heating up said first semiconductor chip or substrate and said second semiconductor chip to a temperature at which said low-melting point metal layer melts, to thereby join said substrate and semiconductor chip together (Fig. 6); and wherein one of said first bumps and corresponding second bumps is smaller in diameter than the other (Fig. 5, the first bump 20 is smaller in diameter than the second bump 38), and said first and corresponding second bumps are joined by heating such that a fillet is formed and covers at least part of a side wall of the smaller of said first and corresponding second bump (Fig. 5, 43). Dalal does not teach that the semiconductor chip and substrate are superposed without perfect alignment, that the chip and substrate are self-aligned upon heating. Call teaches that a chip and semiconductor are misaligned, and then self-align upon

the heating and melting of solder bumps (Col 1 Ln 42-46). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the bumps of Dalal self-align as taught by Call in order to compensate for the chip's misalignment. Furthermore, Dalal does not teach that said first and corresponding second bumps have ends that are substantially flat. Akamatsu teaches first and second bumps having ends that are substantially flat (Fig. 1, 3 and 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide flat ends on the bumps of Dalal as taught by Akamatsu in order to ensure that the electrical connection has a low contact resistance and is free from repellency problems.

Furthermore, Dalal does not teach that at least one of said first or second bumps is a tin layer having a thickness of about 0.1 to 4 micrometers, said at least one of said first or second bumps being made of gold. Scharr teaches a tin layer having a thickness between 0.1 to 4 micrometers (Col 2 Ln 53), and that at least one of a first and second bump is made of gold (Fig. 2, 28). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a bump of gold and a tin layer of 0.1 to 4 micrometers as taught by Scharr in order to form a gold-tin eutectic, which does not compromise the high frequency performance of the device (Col 4 Ln 5).

Furthermore, Dalal and Call do not teach that said insulating resin has a thermal shrinkage factor of 4% or less. Bando teaches a thermosetting setting resin having a shrinkage factor of 3% (Col 3 Ln 56). It would have been obvious

to one of ordinary skill in the art at the time the invention was made to use a resin having a thermal shrinkage factor of 4% or less as taught by Bando in order to avoid volume reduction upon curing.

Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dalal, Call, Scharr, Bando, and Akamatsu, in view of Yamada et al (U.S. Patent #5864178), further in view of the admitted prior art in the applicant's specification.

With respect to **claim 34**, Dalal teaches gold bumps (Col 8 Ln 55), but Dalal and Call do not teach that said insulating resin and said first and second bumps have approximately the same elastic modulus. Yamada teaches a polyimide resin (Col 22 Ln 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a resin in the device of Dalal as taught by Yamada in order to reduce the mechanical stress in the device. Furthermore, the applicant's specification discloses that polyimide resin has approximately the same elastic modulus as gold bumps (Paragraph 80). It would have been obvious to one of ordinary skill in the art to have first and second bumps having approximately the same elastic modulus of the insulating resin because it is a normal property of each material.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben P. Sandvik whose telephone number is (571) 272-8446. The examiner can normally be reached on Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571)272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

bps

EVAN PERT
PRIMARY EXAMINER